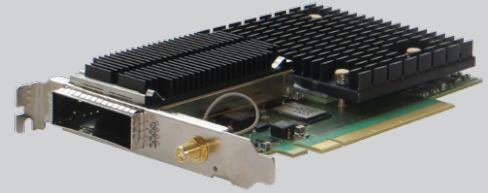




A Silicom Company



fb2CG@V7580

The fb2CG@V7580 is a high performance OEM hardware platform intended for 100G Ethernet with CFP4 network interface.

The standard configuration is based on Xilinx Virtex7 H580T FPGA. The card is also offered with a variety of different FPGAs to provide flexibility for the intended application.

HOST INTERFACE

- Physical bus connector: 16-lane PCIe
- PCIe bus type: 1-8 lane PCIe Gen1/Gen2/Gen3
- Support up to 2 x 8 lane bifurcation PCIe Gen3

NETWORK INTERFACE

- IEEE 802.3 100 Gbit/s Ethernet
- Physical interface: 2 x CFP4 port
- Supported CFP4 modules: Including fan-out modules for 4 x 25 G, Multimode SR (850 nm), singlemode LR (1 31 0 nm), multimode LRM (1 31 0 nm), or Direct Attached Copper (Twinax)
- Data rate: 100 Gbit/s or 4 x 25 Gbit/s
- Ethernet PHY directly embedded in FPGA

CONFIGURATION

- 16 bit fast parallel programming interface from supporting preprogrammed controller
- Configuration flash supports two boot images with automatic fallback to fail safe image if first image fails
- Upload of FPGA configuration to flash via PCIe
- Support for encrypted FPGA bit file (optional)

ON BOARD MEMORY

- 3 x 64 bit DDR3@1800MT/s 4GB (12 MB in total)
- 1 MB user configurable space in flash for permanent storage

ON BOARD CLOCK

- PCIe clock: 100MHz
- 125 MHz oscillator
- 156.25 MHz oscillator
- 322.265625 MHz oscillator

CARD/FPGA VERSIONS AVAILABLE

- fb2CG@V7580: Xilinx Virtex7 XC7VH580T-2
- Xilinx Virtex7 XC7VH580T-3 (optional)
- Xilinx Virtex7 XC7VH870T-2 (optional)
- Other speedgrades available on request

ENVIRONMENT

- Physical dimensions: Half length, standard height PCIe
- Power consumption: Less than 7W with uninitialized FPGA
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE
- Passive cooling (no on-board fan required)
- Active cooling (optional)

ADDITIONAL BOARD SUPPORT

- On board temperature sensor
- Board status LED
- 8 user FPGA controlled dual color LED for Link/Activity and other status
- PPS clock synchronization connector

ADDITIONAL INTELLECTUAL PROPERTY MODULES

- Flash configuration I/F
- DDR3 memory controller
- 8 lane PCIe
- DMA for 2 x 8 lanes Gen3 (optional)
- 100G Ethernet MAC and PCS/PMA (optional)
- MDIO controller (optional)
- I2C controller (optional)
- SPI master I/F (optional)
- TCP-offload engine (optional)

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