Silicom Denmark A/S
FPGA SOLUTIONS

fbSmartNIC2.0

for time critical communication

The fbSmartNIC2.0 product is designed to competitively enhance performance in a host of networking, financial and big data solutions. It consists of highly optimised functionality well suited for e.g. financial algorithmic trading platforms where sub-micro second latency is crucial.

Complete transport layer offload can be combined with customised logic directly implemented in the powerful on-board FPGA. It comes with a full software API for seamless integration and monitoring. fbSmartNIC 2.0 is available on stock from Silicom Denmark.

HOST INTERFACE
- Physical bus connector: 16-lane PCIe
- Supported bus type: 1-16 lane PCIe Gen1/Gen2/Gen3
- PCIe compliant

TIME STAMPING & SYNC
- External synchronization: PPS
- Daisy chain between multiple cards supported

NETWORK INTERFACE
- IEEE standard: IEEE 802.3 10/40/25/100 GE
- Physical interface: 4 x QSFP28 ports
- Supports QSFP+/QSFP28 modules: including fan-out modules for 4x10G/4x25GE per slot, Multimode SR4 (850nm), singlemode LR4 (1310nm), singlemode PSM4 (1310nm), multimode LRM4 (1310 nm), or Direct Attached Copper (Twinax) and others
- Data rate: 16 x 10 Gbit/s
- Ethernet PHY directly embedded in FPGA

CONFIGURATION
- 16-bit fast parallel programming interface from supporting preprogrammed controller
- Configuration flash supports two boot images with automatic fallback to fail safe image if first image fails
- Upload of FPGA configuration to flash via PCIe

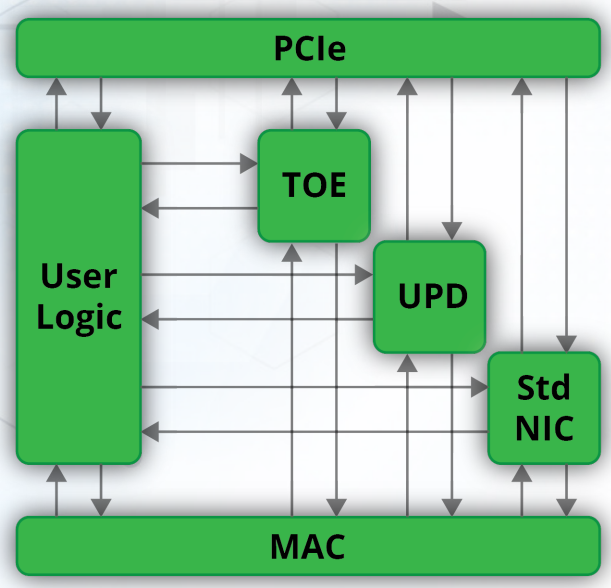
ON BOARD MEMORY
- 2 x 64-bit DDR4@2400MT/s 4GB
  - » 64-bit DDR4 @2133MT/s 4 GB
  - » 36-bit QDRII+ @1266MT/s 288 Mb
  - » 36-bit SQIVe/QDRIV @1600MT/s 288 Mb

ON BOARD CLOCK
- PCIe clock: 100MHz
- 200 MHz clock
- 50 MHz clock
- 161.13 MHz clock

FPGA VERSION
- fb4CGg3@VU09P: Virtex Ultrascale+ XCVU9P

ENVIRONMENT
- Physical dimensions: 3/4 length, standard height PCIe
- Power consumption <10W with uninitialized FPGA
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE
- Active cooling (heat sink with fan)
- Passive cooling (optional)

ADDITIONAL BOARD SUPPORT
- On-board power and temperature sensors
- Board status LED
- User configurable dual color LED
- FPGA controlled Link and Activity LED for each port
- External clock synchronization connector
- PCIe AUX power connector and cable



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Dedication to Performance

Silicom Denmark A/S
FPGA SOLUTIONS

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The fbSmartNIC framework is designed to enhance performance in a host of networking, financial and big data scenarios. Key benefits include increased throughput with zero data loss without interruption of server processes. Business opportunities such as e.g. High Frequency Trading and High Volume Data Collection systems can benefit substantially from this complete hardware off-loading of TCP/UDP communication. It includes market leading TOE (TCP Offload Engine) and UOE (UDP Offload Engine) as well as a highly optimised MAC layer. The fbSmartNIC framework supports various Silicom Denmark cards featuring technologies such as Xilinx, Altera and ZYNQ.

LATENCY
- Wire to wire latency of 455 ns: Receiving on UDP port, through User Logic, and sending from TCP port
- Full 10G throughput on TCP port

MAC
- Combined MAC (10GbE) and PCS (10GBA-SE-R) IP core
- Fixed latency of 67 ns: User Logic to wire, Tx + Rx

PERFORMANCE
- Data rate: 10 Gbit/s
- TCP/UDP throughput at line rate

UDP OFFLOAD ENGINE
- 64 UDP multicast streams accessible to Host and User Logic
- Configurable to any single available port
- IGMP support

TCP OFFLOAD ENGINE (TOE)
- Up to 64 TCP connections accessible to Host and User Logic
- Configurable to any available port

USER LOGIC
- 8 dedicated DMA Channels to/from Host System at full PCIe speed
- 1 MB of register access
- All TCP and UDP streams accessible
- Access to all physical ports

STANDARD NIC full
- Standard NIC Support
- Configurable to all available ports running alongside TOE and UDP Engine
- Data path also accessible to User Logic

SOFTWARE API
- Multi DMA channel streaming (128 channels) with host dependent DMA buffer
- C based API (DLL/Shared library) Linux (Windows & FreeBSD on request)

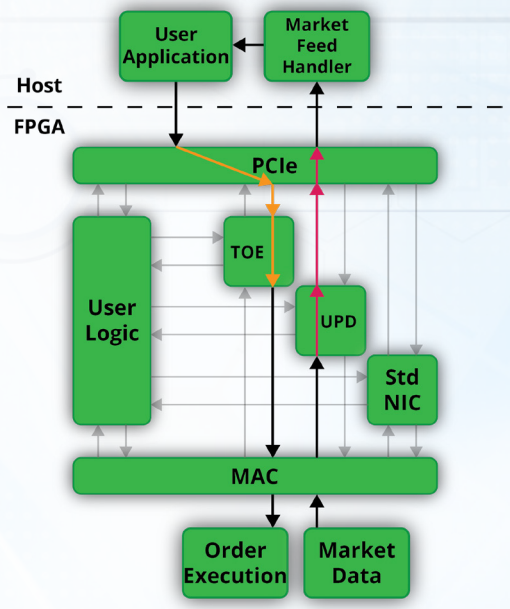
TIME STAMPING & SYNC
- Resolution = 1 ns
- Accuracy down to 20 ns

ENVIRONMENT
- At 3/4 of the FPGA resources are available for User Logic

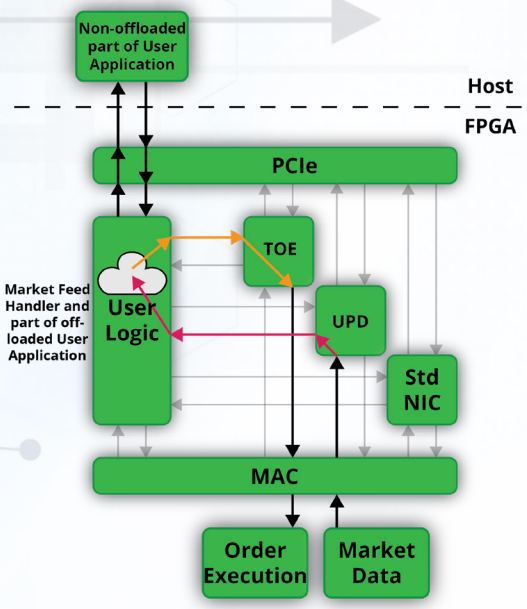
ON-BOARD SENSOR READINGS
- Current fbSmartNIC2.0 System status available in Software API
- Temperature with present minimum, maximum card operating temperature
- Link status
- TCP State information

STATISTICS
- Statistics are based on a subset of RFC2819 RMON1
- Statistics are provided on a per second basis
- Network counter: Number of Octet, CRC Align Errors, Undersize Packets, Oversize Packets, Jabbers, etc.

TCP and UDP accelerated Trading Scenario



TCP and UDP accelerated Trading Scenario with Market Feed Handler and Order Execution in User Logic



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