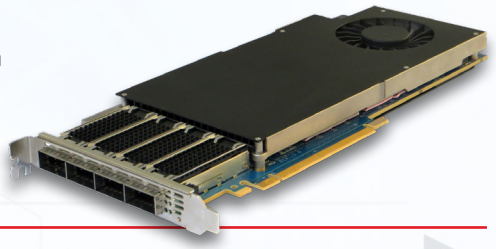
Silicom Denmark A/S
FPGA SOLUTIONS

fb4CGg4 @VU09P



Silicom's Xilinx® FPGA SDAccel 10/25/40/50/100 Gigabit compatible server adapter is based on a high performance Xilinx® FPGA UltraScale+. Silicom's FPGA SDAccel adapter has the same 'out of box' experience as the Xilinx® VCU1525 development kit, currently used for VU9P based SDAccel based solutions. This will enable all customer designs, SDAccel platform source files and examples to be seamlessly migrated to this card.

The SDAccel™ development environment for OpenCL™, C, and C++, enables up to 25X better performance/watt for data center application acceleration leveraging FPGAs. SDAccel, member of the SDx™ family, combines the industry's first architecturally optimizing compiler supporting any combination of OpenCL, C, and C++ kernels, along with libraries, development boards and the first complete CPU/GPU like development and run-time experience for FPGAs.

SDAccel™ is a development environment for OpenCL™ applications targeting Xilinx® FPGA-based accelerator cards. This environment enables concurrent programming of the in-system processor and the FPGA fabric without the need for RTL design experience. The application is captured as a host program written in C/C++ and a set of computation kernels expressed in C, C++, or the OpenCL C language.

HOST INTERFACE

- Physical bus connector: 16-lane PCIe
- PCIe bus type: 1-16 lane PCIe Gen1/Gen2/Gen3

NETWORK INTERFACE

- IEEE standard: IEEE 802.3 10/40/25/100 GE
- Physical interface: 4 x QSFP28 ports
- Supports QSFP+/QSFP28 modules: including fan-out modules for 4x10G/4x25GE per slot, Multimode SR4 (850nm), singlemode LR4 (1310nm), singlemode PSM4 (1310nm), multimode LRM4 (1310 nm), or Direct Attached Copper (Twinax) and others
- Data rate: 16x10, 4x40, 16x25, 4x100 Gbps

CONFIGURATION

- Quad SPI parallel programming interface from supporting preprogrammed controller
- Configuration flash supports two boot images
- Upload of FPGA configuration to flash via PCIe or directly from Xilinx® Vivado via the on-board Jtag dongle
- Direct FPGA configuration from Xilinx® Vivado via the on-board Jtag dongle

ON-BOARD MEMORY

- DDR4 with ECC
  - » 4 x 72-bit DDR4@2133MT/s 16GB pr. bank
- 2 x 1Gb Quad SPI flash for dual FPGA configurations
- 8Kb I2c EEPROM user configurable

ON-BOARD CLOCK

- PCIe clock: 100 MHz
- 4 x differential 300 MHz clock for memory interfaces
- 4 x differential 161.13 MHz SerDes clock (can be changed to 156.25 MHz)
- 4 x differential 156.25 MHz SerDes clock (can be configured in variable steps)
- Differential 90 MHz user clock

FPGA DETAILS

- Xilinx® UltraScale+ XCVU9P, 16nm, Package D2104

ENVIRONMENT

- Physical dimensions: Full height, ¾ length, 111.15 x 254 mm with bracket
- PCI Express voltage: +12V ± 8% and 3.3Vaux optionally
- Hardware compliance: RoHS, CE
- Active heat sink, targeted to single socket
- Passive heat sink, targeted to dual slot
- Built-in thermal protection

ADDITIONAL BOARD SUPPORT

- On-board power and temperature sensors
- Board status LED
- User configurable triple color LED
- On board auxiliary power connector to support power over 75W

ORDERING INFORMATION

fb4CGg4@VU09P-2-H	Passive cooling
fb4CGg4@VU09P-2-A	Active cooling

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Dedication to Performance