



### FB4CGG5@VU09P TimeSync FPGA Card

#### Quad Port QSFP28 100 Gigabit FPGA Card

#### Product Description

The FB4CGG5@VU09P TimeSync is a high-performance OEM hardware platform intended for 10/40/25/100 Gigabit Ethernet via its quad QSFP28 slots.

The card supports various FPGA models, and in its standard version it is fitted with an AMD® Virtex UltraScale+ VU9P FPGA SG3, to provide ample capacity for the quad QSFP28 interface.

The card is mounted with 2 x 64-bit DDR4 2400MT/s 4GB for a total of 8 GB. In addition to this it features 2 SODIMM sockets for use with DDR4 or QDR11+ modules for low latency applications.

The card features the ZL30793 DPLL for optimal clock control, allowing compliance with IEEE-1588-2019 SyncE and PTP.



#### Key Features

- AMD® Virtex UltraScale+ VU9P FPGA
- 4 x QSFP28 ports
- DPLL ZL30793
- 2 x 64-bit DDR4@2400MT/s
- 2 x SODIMM for optional QDR11+ or extra DDR4
- Configuration flash RAM for boot images
- PCIe form-factor: 3/4 length, standard height PCIe
- On-board power and temperature sensors
- FPGA controlled link and status LEDs
- Passive cooling (optional)



#### Technical Specifications

Network Interface	
IEEE standard	IEEE 802.3 10GE, 40GE, 25GE, 100GE
Interfaces	<ul style="list-style-type: none"> <li>▪ Physical interface: 4 x QSFP28 slots (2 port variant available)</li> <li>▪ Supports QSFP+/QSFP28 modules: including fan-out modules for 4x10G/4x25GE per slot, Multimode SR4 (850nm), singlemode LR4 (1310nm), singlemode PSM4 (1310nm), multimode LRM4 (1310 nm), or Direct Attached Copper (Twinax) and others</li> <li>▪ Data rate: 16x10, 4x40, 16x25, 4x100 Gbps</li> </ul>
Host Interface	
PCI bus	<ul style="list-style-type: none"> <li>▪ 16 lanes PCIe Gen1/Gen2/Gen3</li> <li>▪ PCIe compliant</li> </ul>

General Technical Specifications	
<b>Configuration</b>	<ul style="list-style-type: none"> <li>▪ 16-bit fast parallel programming interface from supporting preprogrammed controller</li> <li>▪ Configuration flash supports two boot images with automatic fallback to fail safe image if first image fails to load</li> <li>▪ Upload of FPGA configuration to flash via PCIe</li> <li>▪ Support for encrypted FGPA bit file (optional)</li> </ul>
<b>On-board Memory</b>	<ul style="list-style-type: none"> <li>▪ 2 x 64-bit DDR4@2400MT/s 4 GB</li> <li>▪ 2 x Optional SODIMM <ul style="list-style-type: none"> <li>• 64-bit DDR4 @2400MT/s 4 GB</li> <li>• 36-bit QDRII+ @1266MT/s 288 Mb</li> </ul> </li> <li>▪ 8 MB user configurable space in flash RAM for permanent storage</li> <li>▪ 256 MB Configuration flash RAM for boot images</li> </ul>
<b>On-board Clock</b>	<ul style="list-style-type: none"> <li>▪ PCIe clock: 100 MHz</li> <li>▪ 200 MHz clock</li> <li>▪ 50 MHz clock</li> <li>▪ 161.13 MHz clock</li> <li>▪ DPLL ZL30793</li> </ul>
<b>FPGA Details</b>	<ul style="list-style-type: none"> <li>▪ AMD® Virtex UltraScale+ VU09P</li> <li>▪ Other options can be provided</li> </ul>
<b>Environment</b>	<ul style="list-style-type: none"> <li>▪ Physical dimensions: 3/4 length, standard height PCIe</li> <li>▪ Power consumption: &lt;10W with uninitialized FPGA</li> <li>▪ Operating temperature: 0 – 55°C, 30 – 130°F</li> <li>▪ Operating humidity: 20 – 80%</li> <li>▪ Hardware compliance: RoHS, CE</li> <li>▪ Active cooling (heat sink with fan)</li> <li>▪ Passive cooling (optional)</li> </ul>
<b>Additional Board Support</b>	<ul style="list-style-type: none"> <li>▪ On-board power and temperature sensors</li> <li>▪ Board status LEDs</li> <li>▪ User configurable dual color LED</li> <li>▪ FPGA controlled Link and Activity LED for each port</li> <li>▪ PPS clock synchronization connector</li> <li>▪ PCIe AUX power connector and cable</li> </ul>
<b>Time Synchronization</b>	<ul style="list-style-type: none"> <li>▪ PTP: Yes, with PTP4L or zlsptp on x86</li> <li>▪ Support Sync-E/ 1588 standard</li> <li>▪ DPLL: ZL30793</li> </ul>
<b>Additional Intellectual Property Modules</b>	<ul style="list-style-type: none"> <li>▪ PacketMover framework (optional)</li> <li>▪ SmartNIC framework (optional)</li> <li>▪ Ultra-low latency 10GE MAC (optional)</li> <li>▪ TCP-offload engine (optional)</li> </ul>
<b>Ordering Example</b>	<p><i>FB4CGG5@VU09P-3-RR-1A</i>  4-port card with the following configuration:</p> <ul style="list-style-type: none"> <li>▪ VU09P Virtex UltraScale+ FPGA</li> <li>▪ Speedgrade -3 (fastest available)</li> <li>▪ 288 Mb x36 QDRII+ RAM mounted in SoDimm slot A</li> <li>▪ 288 Mb x36 QDRII+ RAM mounted in SoDimm slot B</li> <li>▪ SMA connector for PPS signal on front panel</li> <li>▪ Heat sink with integrated UL/CE approved fan</li> </ul>

## Ordering Guide

**FB4CGG5@** -- (Quad QSFP28/QSFP+)

**FB2CGG5@** -- (Dual QSFP28/QSFP+)

### FPGA Type

VU05P = Virtex VU5P  
 VU07P = Virtex VU7P  
 VU09P = Virtex VU9P \*  
 VU11P = Virtex VU11P  
 VU13P = Virtex VU13P  
 VU080 = Virtex VU80  
 VU095 = Virtex VU095  
 VU125 = Virtex VU125  
 VU160 = Virtex VU160  
 VU190 = Virtex VU190  
 KU095 = Kintex KU95  
 KU115 = Kintex KU115

### Speedgrade

1 = Speedgrade 1  
 2 = Speedgrade 2\*  
 3 = Speedgrade 3

### Cooling

P = Passive  
 A = Active\*

### PPS clock IO

0 = Not installed  
 1 = SMA connector installed\*

### SODIMM B

0 = No SODIMM RAM installed\*  
 R = QDRII+ RAM installed (x36, 288 Mb)

### SODIMM A

R = QDRII+ RAM installed (x36, 288 Mb)  
 D = DDR4 RAM installed (x64, 4 GB)

### \* Default configuration

<b>Ordering Information</b>	FB4CGG5@VU09P-2-00-1A	Virtex UltraScale+ VU9P-2, No SODIMMs
	FB4CGG5@VU09P-2-DD-1A	Virtex UltraScale+ VU9P-2, 2x4GB DDR4 SODIMMs
	FB4CGG5@VU09P-2-RR-1A	Virtex UltraScale+ VU9P-2, 2xQDRII RAM (x36, 288Mb)
	FB4CGG5@VU09P-3-00-1A	Virtex UltraScale+ VU9P-3, No SODIMMs
	FB4CGG5@VU09P-3-DD-1A	Virtex UltraScale+ VU9P-3, 2x4GB DDR4 SODIMMs
	FB4CGG5@VU09P-3-RR-1A	Virtex UltraScale+ VU9P-3, 2xQDRII RAM (x36, 288Mb)

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### www.silicom-usa.com

Silicom Ltd.  
 International Headquarters  
 14 Atir Yeda St.  
 Kfar Sava 4464323  
 Israel  
 Tel: (972)-9-764-4555

Silicom Connectivity Solutions Inc.  
 USA Office  
 6 Forest Ave, Paramus  
 New Jersey 07652  
 USA  
 Tel: 18004silicom (Toll Free no.)

### www.silicom.dk

Silicom Denmark A/S  
 Poppelgaardvej 11  
 DK-2860 Soeborg  
 Denmark  
 Phone +45 46 32 74 55  
 contactus@silicom.dk