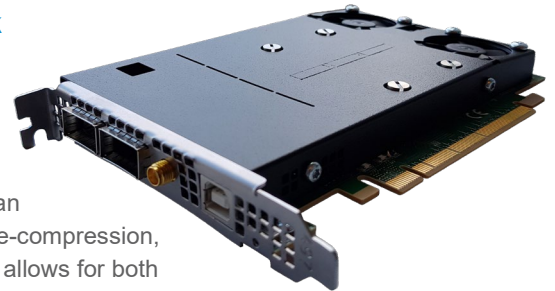




## PacketMover - FPGA acceleration and development framework

Silicom's PacketMover is an FPGA framework, designed for simplifying development and integration of offload functions, acceleration, and applications for up to 100GE networking, as well as for pure compute tasks. Applications and compute tasks demanding the highest performance and flexibility only an FPGA can provide. Typical tasks include heavy computational tasks such as: Compression/de-compression, Encryption/ decryption, Data slicing, Deep Packet Inspection (RegEx). The design allows for both inline and monitoring solutions.

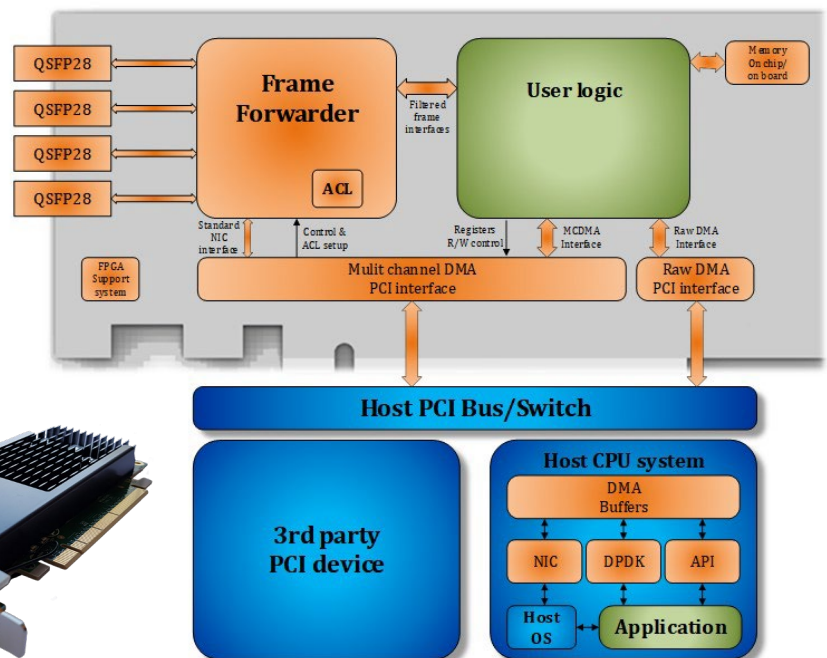
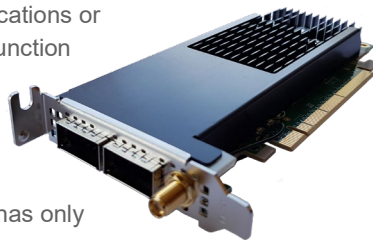


PacketMover is offering a platform bridging the gap between high-performance applications and cutting edge hardware. Through the use of Silicom's world class FPGA accelerator boards, reconfigurable computing is within the grasp of system designers and integrators.

PacketMover provides an abstraction of the hardware for development of custom applications in FPGA. The PacketMover framework itself is only consuming a small amount of FPGA resources leaving the vast majority of resources for the Custom Packet Processor. The sandbox for the offload function or custom application. Using standardized interfaces, PacketMover ensures easy fit of custom and standard IP blocks.

The framework manages a number of complex interface, removing the complexity of dealing directly with the Hardware of the network and PCIe. It Provides packets to the Custom Packet Processor or directly to Host side applications. Even the PCIe interface is managed by a multichannel DMA system, providing flexible arbitration of multiple channels, which can be split between different host side interfaces such as Standard NIC, DPDK and API controlled buffers on the host. Even towards 3rd party PCIe device, such as a GPU to keep the host CPU free to other tasks then task suitable for offloading.

With DPDK support, many industry standard storage and analysis applications can directly connect to the high performance application built within the FPGA Custom Packet Processor. The built-in standard NIC function allows the FPGA card to double as a standard network interface for applications or platform traffic, in parallel or in conjunction with FPGA based custom application. Through the included API, access into the DMA buffers for optimal performance can be achieved as it has only minimal impact on host CPU resources.



The Frame forwarder of the framework offer accurate timestamping and manages the Rx and Tx of the solution. It features an Access Control List function, allowing it to direct data toward the Custom Packet Processor or to even bypass it, and send data directly to host or 3rd party PCIe device. Thus ensuring performance resources can be applied optimally.

Controlling applications in PacketMover is very flexible and allows direct communication to the custom function or application through configurations and registers access. The Framework provides accurate traffic and rule match statistics of ports and ACL. Management, deployment and monitoring tool s are provided for ease of use of application built on PacketMover.

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